#3 IDS 11-28-01 R stokes

Docket No. 213672US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Kenji YAMAGUCHI, et al.

SERIAL NO: NEW APPLICATION GAU:

FILED: HEREWITH EXAMINER:

FOR: SEMICONDUCTOR DEVICE EVALUATION METHOD AND APPARATUS, SEMICONDUCTOR DEVICE MANUFACTURING CONTROL METHOD, SEMICONDUCTOR DEVICE MANUFACTURING METHOD, AND RECORDING MEDIUM

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

□ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

■ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.

□ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

□ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

□ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Marvin J. Spivak
Registration No. 24,913

C. Irvin McClelland
Registration Number 21,124

22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/98)

LIST OF RELATED CASES

Docket Number	Serial or Patent No.	Filing or Issue Date	Status or Patentee
0057-2406-2YYX	09/238,887	01/28/99	PENDING
0057-2577-2YY	09/487,826	01/20/00	PENDING

GJM/ae
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IN RE APPLICATION OF: Kenji YAMAGUCHI, et al.

SERIAL NO.: New Application

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FOR: SEMICONDUCTOR DEVICE EVALUATION METHOD AND APPARATUS, SEMICONDUCTOR DEVICE MANUFACTURING CONTROL METHOD, SEMICONDUCTOR DEVICE MANUFACTURING METHOD, AND RECORDING MEDIUM

STATEMENT OF RELEVANCY

Reference AO on Form PTO-1449:

According to the present invention, insulating gate field effect transistors Tr1-Tr6 have a common gate electrode pattern 1, as shown in Fig. 1. The insulating gate field effect transistors Tr1-Tr6 comprise gate electrodes 1a-1f with different design gate lengths, and sources 2 and drains 3, respectively. Each conductance of gate electrodes of transistors Tr1-Tr6 is measured, and a sheet resistance is calculated based on the inclination of a straight line of a region wherein there is a linear relationship between the measured conductance and the design gate lengths of transistors Tr1-Tr6. Further, based on the sheet resistance, a plurality of intervals between terminals and gate electrode conductance, a gate length that is the width of the gate electrode pattern 1 is calculated.

Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 213672US2	SERIAL NO. NEW APPLICATION
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Kenji YAMAGUCHI, et al.	
		FILING DATE HEREWITH	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO	9-92700	4/4/97	Japan		X
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	Narain D. ARORA, et al. "AN ACCURATE METHOD OF DETERMINING MOSFET GATE OVERLAP CAPACITANCE" Solid State Electronics Vol. 35, No. 12, 1992, pgs. 1817-1822
	AX	
	AY	
	AZ	

Examiner	Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.